WHAT IS CLAIMED IS:

1. Circuitry for use with a general purpose performance counter ("GPPC") connected to a bus carrying a plurality of encoded state coverage signals indicative of test coverage in a logic design, said circuitry for decoding and capturing coverage information, comprising:

a selection circuit operating to select said plurality of encoded state coverage signals from a multi-bit event signal carried on said bus;

a line decoder operating to decode said plurality of encoded state coverage signals into *N* one-hot signals, wherein each one-hot signal is asserted when a corresponding state in said logic design is covered during a test; and

a capture circuit coupled to said line decoder for capturing said *N* one-hot signals.

2. The circuitry as recited in claim 1, wherein said capture circuit comprises:

an OR logic block for bit-wise ORing said *N* one-hot signals with an *N*-bit mask value stored in a register block, said OR logic block operating to generate an *N*-bit output; and

a Multiplexer (MUX) block operating to select said *N*-bit output from said OR logic block under control of at least one control signal, wherein said *N*-bit output is operable to be stored into said register block when selected by said MUX block.

3. The circuitry as recited in claim 2, wherein said OR logic block comprises *N* 2-input OR gates.

4. The circuitry as recited in claim 2, wherein said MUX block comprises *N* MUX elements, each for selecting a particular bit of said *N*-bit output.

5. The circuitry as recited in claim 2, wherein said MUX block comprises *N* MUX elements, each operating responsive to two control signals for selecting among four MUX inputs, including a particular bit of said *N*-bit output.

6. The circuitry as recited in claim 5, wherein one of said MUX inputs comprises a value stored in a control status register (CSR).

7. The circuitry as recited in claim 5, wherein one of said MUX inputs comprises said mask value stored in said register block.

8. The circuitry as recited in claim 5, wherein one of said MUX inputs comprises a fixed binary 0 value.

9. The circuitry as recited in claim 1, wherein *N* is 80.

10. A method of capturing state coverage information in a logic design, comprising:

encoding state coverage information generated when said logic design is exercised under test onto a segment of a bus connected to a general purpose performance counter ("GPPC");

selecting said segment of said bus for processing;

decoding said segment of said bus into *N* one-hot signals, wherein each one-hot signal is asserted when a corresponding state in said logic design has been covered during test;

bit-wise ORing said *N* one-hot signals with an *N*-bit mask value stored in a register block for generating an *N*-bit output; and

selecting said *N*-bit output by a Multiplexer (MUX) block operating under control of at least one control signal, wherein said *N*-bit output is operable to be stored into said register block when selected by said MUX block.

11. The method of capturing state coverage information in a logic design as recited in claim 10, wherein said bit-wise ORing operation is performed by an OR logic block comprising *N* 2-input OR gates.

12. The method of capturing state coverage information in a logic design as recited in claim 10, wherein said selecting of said *N*-bit output is performed by a MUX block comprising *N* MUX elements, each operating responsive to two control signals for selecting among four MUX inputs, including a particular bit of said *N*-bit output.

13. The method of capturing state coverage information in a logic design as recited in claim 12, wherein one of said MUX inputs comprises a value stored in a control status register (CSR).

14. The method of capturing state coverage information in a logic design as recited in claim 12, wherein one of said MUX inputs comprises said mask value stored in said register block.

15. The method of capturing state coverage information in a logic design as recited in claim 12, wherein one of said MUX inputs comprises a fixed binary 0 value.

16. The method of capturing state coverage information in a logic design as recited in claim 10, wherein N is 80.

17. A system for capturing state coverage information in a logic design, comprising:

means for encoding state coverage information generated when said logic design is exercised under test onto a segment of bus connected to a general purpose performance counter ("GPPC");

means for selecting said segment of said bus for processing;

means for decoding said segment of said bus into *N* one-hot signals, wherein each one-hot signal is asserted when a corresponding state in said logic design has been covered during test;

means for generating an *N*-bit output based on a logic operation between said *N* one-hot signals and an *N*-bit mask value stored in a register block; and

a Multiplexer (MUX) block operating to select said *N*-bit output under control of at least one control signal, wherein said *N*-bit output is operable to be stored into said register block when selected by said MUX block.

18. The system for capturing state coverage information in a logic design as recited in claim 17, wherein said means for generating said *N*-bit output comprises an OR logic block that includes *N* 2-input OR gates for performing a bit-wise logic OR operation.

19. The system for capturing state coverage information in a logic design as recited in claim 17, wherein said MUX block comprises *N* MUX elements, each operating in response to two control signals for selecting among four MUX inputs, including a particular bit of said *N*-bit output.

20. The system for capturing state coverage information in a logic design as recited in claim 19, wherein one of said MUX inputs comprises a value stored in a control status register (CSR).

21. The system for capturing state coverage information in a logic design as recited in claim 19, wherein one of said MUX inputs comprises said mask value stored in said register block.

22. The system for capturing state coverage information in a logic design as recited in claim 19, wherein one of said MUX inputs comprises a fixed binary 0 value.

23. The system for capturing state coverage information in a logic design as recited in claim 17, wherein N is 80.